

Compiling for the Molen Programming Paradigm

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1 Introduction

In the last decade, several approaches have been proposed for coupling an FPGA to a GPP. For a classification of these approaches the interested reader is referred to [4]. There are four shortcomings of current approaches, namely:

1. **Opcode space explosion:** a common approach (e.g. [2], [3]) is to introduce a new instruction for each part of application mapped into the FPGA. The consequence is the limitation of the number of operations implemented into the FPGA, due to the limitation of the opcode space.
2. **Limitation of the number of parameters:** In a number of approaches, the operations mapped on an FPGA can only have a small number of input and output parameters ([1], [6]), due to the encoding limits.
3. No support for **parallel execution** on the FPGA of sequential operations: an important and powerful feature of FPGA's can be the parallel execution of sequential operations when they have no data dependency. Many architectures [4] do not take into account this issue and their mechanism for FPGA integration cannot be extended to support parallelism.
4. No **modularity:** each approach has a specific definition and implementation bounded for a specific reconfigurable technology and design. Consequently, the applications cannot be (easily) ported to a new reconfigurable platform. Further there are no mechanisms allowing reconfigurable implementation to be developed separately and ported transparently.

A general approach is required that eliminates these shortcomings. In this paper, a programming paradigm for reconfigurable architectures [5], called the Molen Programming Paradigm and a compiler are described that offer alternatives and a solution to the above presented limitations.

2 The Programming Paradigm

The Molen programming paradigm[5] is a sequential consistency paradigm for programming CCMs possibly including a general purpose computational engine(s). The paradigm allows for parallel and concurrent hardware execution and it is intended (currently) for single program execution. It requires only a one time architectural extension of few instructions to provide a large user reconfigurable operation space. The added instructions (currently supported by the compiler) include:

- Two instructions¹ for controlling the reconfigurable hardware, namely:
 - SET *< address >*: at a particular location the hardware configuration logic is defined
 - EXECUTE *< address >*: for controlling the executions of the operations on the reconfigurable hardware
- Two move instructions for passing values to and from the GPP register file (GPR) and XRs. hardware.

Code fragments constituted of contiguous statements (as they are represented in high-level programming languages) can be isolated as generally implementable functions (that is code with multiple identifiable input/output values). The parameters stored in registers are passed to special reconfigurable hardware registers denoted as Exchange Registers(XRs).

3 Compiler Extensions

The compiler system relies on the Stanford SUIF2 (Stanford University Intermediate Format) Compiler Infrastructure for the front-end, while the back-end is built over the framework offered by the Harvard Machine SUIF. The last component has been designed

¹Actually, five if partial reconfiguration, pre-loading of reconfiguration and executing microcode are explicitly assumed [5].

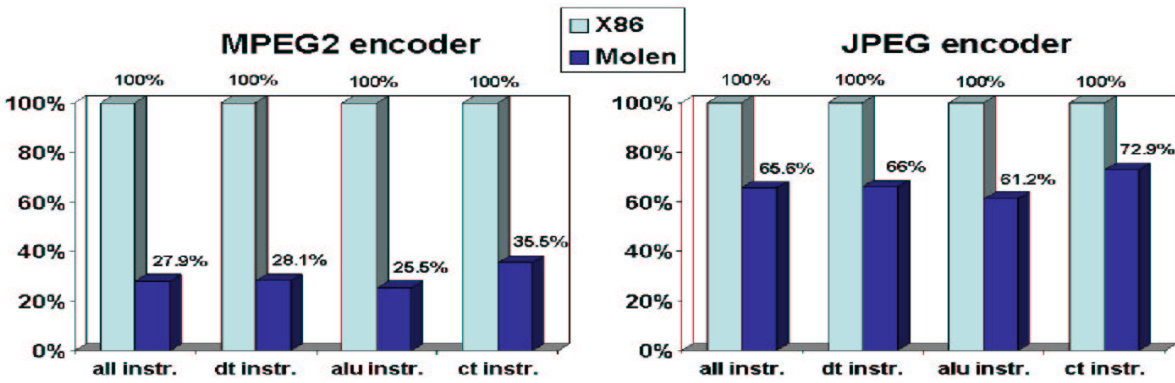


Figure 2. mpeg2enc and jpeg encoder instruction results

Fct	Cycles	% Total
SAD	149.947.461	55.2 %
DCT	42.529.647	15.7 %
VLC	3.946.954	1.4 %
IDCT	3.693.986	1.36 %
mpeg2enc Application	271.616.655	100 %

Table 1. The mpeg2enc (cycles) results

tation of one operation.

The measured data for the GPP alone and the computed data for the Molen processor are compared for mpeg2enc and jpeg in Figure 2. The most important categories of instructions have been considered, namely data transfer (dt) instructions, arithmetic and logical (alu) instructions and control transfer(ct) instructions. From these pictures, a substantial reduction of the number of instructions is achieved by the Molen reconfigurable processor compared to the GPP: 72.1% for mpeg2enc and 34.4 % for jpeg encoder. Also it is obvious that in both cases the alu instructions are the most reduced category of instructions, while the ct instructions are the least reduced instructions. In Table 1 and 2, the cycle measurements are reported. From these results, we can identify those functions that potentially give the highest performance improvement, given an efficient hardware implementation. The numbers suggest that the SAD function is the most promising candidate for hardware implementation, while the rest of the functions can provide at best a moderate performance improvement.

5 Conclusions

The compiler extensions allow to generate code where the operations implemented on the reconfigurable hardware are automatically (rather than manually) substituted by the appropriate SET-EXECUTE instructions. It has been shown through experimentation that the compiler can be used as an important tool

Fct	Cycles	%Total
DCT	40.206.773	12.5 %
VLC	36.571.622	10.5 %
jpeg enc Application	341.316.466	100 %

Table 2. The jpeg encoder (cycles) results

to support the design process focusing on the identification of good candidates for the reconfigurable hardware implementation. The presented results show a substantial reduction of the executed number of instructions and potential reduction of processor cycles for two multimedia benchmarks for their execution on the Molen reconfigurable processor compared to their pure software implementation on the GPP.

References

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